REMARKS

Examiner W.D. Coleman is thanked for the thorough examination and search of the subject Patent Application.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-24 rejected under 35 U.S.C. 103(a) as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) is requested based on the following remarks.

Applicant respectfully disagrees that Dasse et al, in view of Pierrat, teaches or suggestes the key elements of Applicant's method, as described in the claimed invention, such that it would have been obvious to one skilled in the art at the time of the invention to practice Applicant's invention.

Specifically, Applicant's Claim 1 reads:

1. (Original) A method of detecting a reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device.

Of particular importance, Applicant's claimed invention teaches a specific method to actually read or to detect the presence/non-presence of a reticle option layer (lines 19-22).

Claim 1 teaches (1) setting up two transistors on the same IC (lines 3-4 and 9-10 show two transistors are on same IC) where the first transistor is not exposed to a parameter changing process step (lines 8-10) and the second transistor is exposed to a parameter changing process step depending on the use of or non-use of an optional reticle (lines 16-18); (2) measuring the current through the first transistor at a drain test voltage (lines 3-5) and measuring the current through a second transistor at the same drain test voltage (lines 11-13); then (3) comparing the current performance of the two transistors (lines 19-21); and finally (4) deducing the presence or absence of the reticle option based on this comparison (line 21-22). A similar analysis of independent Claims 10, 15, and 20 reveals that each of these claims contains all of the above key features found in Claim 1.

By comparison, Dasse and/or Pierrat do not teach or suggest any of these key features of the reticle detection method of the claimed invention. While Dasse does discuss programming transistors (col. 8), **Dasse does not disclose any method to actually read the programmed transistors.** No where does Dasse disclose, hint, or suggest how to read the "unique codes" present on the NV transistors. Dasse does, indeed, make a reference to "parametric testing" in another section (col. 5,

lines 65-68 and col. 6, lines 1-9). However, there is no contextual tie between the subject matter in the "parametric testing" section (col. 5, lines 65-68 and col. 6, lines 1-9) and the section (col. 8, lines 18-48) discussing ID codes. Specifically, the "parametric testing" section (col. 5, lines 65-68 and col. 6, lines 1-9) of Dasse reads:

"There are two broad categories of electrical tests which can be performed on an integrated circuit die. The first category is functional tests. Functional tests are used to verify the logical functionality of the die independent of timing, AC characteristics, current and voltage levels, or other parametric values associated with the integrated circuit die. This test ensures that an adder adds, a multiplier multiplies, a bus using controls the bus, a memory stores bits properly, etc. The second category is parametric tests. Parametric tests are used to measure integrated circuit die characteristics over a continuous range of inputs parameters, such as voltage, current, timing, power, etc."

The first category of tests - functional, does not apply to Applicant's claimed invention because Dasse makes it clear that these tests "are used to **verify the logical functionality** of the die **independent of** timing, AC characteristics, current and

voltage levels, or other **parametric values. . .**" The present invention teaches testing for a difference between parametric values and then using this difference to determine the presence/absence of a reticle option. Therefore, if anything, the functional test concept teaches against the method of Applicant's claimed invention.

The second category of tests - parametric testing - teaches measuring "integrated circuit die **characteristics** over a continuous range of inputs parameters, **such as voltage, current, timing, power,** etc." Applicant admits that such parametric testing of an IC is well-known in the art. Dasse is merely stating a well-known method of characterizing an IC's performance. However, Dasse does not teach or suggest in this section either the concept of, or the specific method of, performing two parametric tests (measuring current) on two transistors (where each transistor reacts differently to the presence of a reticle option) then comparing the test results and then using the comparison result to determine if the reticle option was or was not used on the IC during processing. This is the method clearly taught in Applicant's claimed invention. Again, there is no contextual tie between Dasse's reference here to parametric testing and Dasse's reference (in col. 8) to

programming an ID code. Dasse simply does not tell us how to read the ID code.

Applicant, therefore, respectfully maintains that the method of determining the presence/absence of a reticle option as described in the claimed invention is not taught or suggested by the cited art such that it would be obvious for one skilled in the art at the time of the invention to practice the invention. Therefore, because the key features of the present invention are not taught or suggested by the cited art, it is respectfully requested that the rejection of Claims 1-24, as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) be removed.

Reconsideration of Claims 1-24 rejected under 35 U.S.C. 103(a) as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) is requested based on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

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Allowance of all Claims is requested.

It is requested that should Examiner W. D. Coleman not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

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